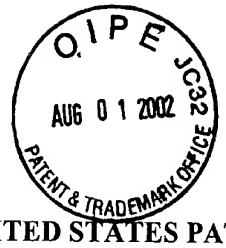

8-2-02

GP 2815

PATENT 8/22/2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Moon et al.

Serial No.: 09/874,631

Filed: June 5, 2001

For: FLEXIBLE BALL GRID ARRAY CHIP SCALE PACKAGES AND METHODS OF FABRICATION

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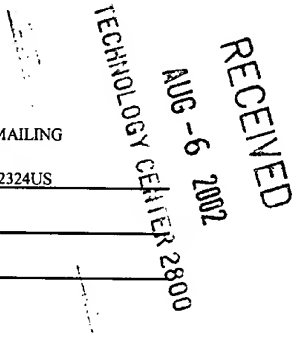

COMMUNICATION

Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is a certified copy of priority document 200102580-8 filed 2 May 2001 for the above-referenced application.

Respectfully submitted,

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Date: August 1, 2002
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Document in ProLaw

REGISTRY OF PATENTS
SINGAPORE

This is to certify that the annexed is a true copy of the following Singapore patent application as filed in this Registry.

Date of Filing	:	2 MAY 2001
Application Number	:	200102580-8
Applicant(s)	:	MICRON TECHNOLOGY, INC.
Title of Invention	:	FLEXIBLE BALL GRID ARRAY CHIP SCALE PACKAGES AND METHODS OF FABRICATION

Yoon Mun Kit
Assistant Registrar
for REGISTRAR OF PATENTS

PATENTS FORM 1

Rule 19

SINGAPORE PATENTS ACT (CHAPTER 221) PATENTS RULES

02 MAY 2001

200102580-8

The Registrar of Patents
Registry of Patents

REQUEST FOR THE GRANT OF A PATENT

THE GRANT OF A PATENT IS REQUESTED BY THE UNDERSIGNED ON THE BASIS OF THE PRESENT APPLICATION

I. Title of Invention	**FLEXIBLE BALL GRID ARRAY CHIP SCALE PACKAGES AND METHODS OF FABRICATION**	
II. Applicant(s) (*See note 2*)	*(a) Name*	**MICRON TECHNOLOGY, INC.**
	Body Description/ Residency	**A CORPORATION OF THE STATE OF DELAWARE, U.S.A.**
	Street Name & Number	**8000 SOUTH FEDERAL WAY BOISE, IDAHO 83707-0006**
	City	
	State	
	Country	**U.S.A.**
	(b) Name	
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	
	(c) Name	
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	

02 MAY 2001
200102580-8

III. Declaration of Priority (see note 3)	Country/Country Designated	U.S.A.	File no.		09/606,432
	Filing Date	28	June	2000	
	Country/Country Designated		File no.		
	Filing Date				
	Country/Country Designated		File no.		
	Filing Date				

IV. Inventors (See note 4)		
(a) The applicant(s) is/are the sole/joint inventor(s).	[ ] Yes [X] Yes	[X] No [ ] No
(b) A statement on Patents Form 8 is/will be furnished.		
V. Name of Agent (if any) (See note 5)	ARTHUR LOKE BERNARD RADA & LEE	

VI. Address for Service (See note 6)	Block/Hse No		Level No	
	Unit No/PO Box	#23-01	Postal Code	038989
	Street Name	9 TEMASEK BOULEVARD		
	Building Name	SUNTEC TOWER TWO		
VII. Claiming an earlier filing date under section 20(3), 26(6) or 47(4). (See note 7)	Application No	N.A.		
	Filing Date			

[Please tick in the relevant space provided]:

( ) Proceeding under rule 27(1)(*a*).

Date on which the earlier application was amended = _____

or

( ) Proceeding under rule 27(1)(*b*).

02 MAY 2001

200102580-8

VIII. Invention has been displayed at an International Exhibition (See note 8)	☐ *Yes* ☒ *No*
IX. Section 114 requirements (See note 9)	The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty. ☐ *Yes* ☒ *No*

X. Check List

(To be filled in by applicant or agent)

A. The application contains the following number of sheet(s):-

1. Request	4	*sheets*
2. Description	15	*sheets*
3. Claim(s).	11	*sheets*
4. Drawing(s).	8	*sheets*
5. Abstract.	1	*sheets*

B. The application as filed is accompanied by:-

1. Priority document	
2. Translation of priority document	
3. Statement of Inventorship & right to grant	X
4. International Exhibition Certificate	

XI. Signature(s)

(See note 10)

Applicant (a)	
Date	2 MAY 2001
Applicant (b)	
Date	
Applicant (c)	
Date	

02 MAY 2001

200102580-8

NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the prescribed fee and 3 copies of the description of the invention, and of any drawings.

2. Enter the name and address of each applicant in the spaces provided at paragraph II. Names of individuals should be indicated in full and the surname or family name should be underlined. The names of all partners in a firm must be given in full. The place of residence of each individual should also be furnished in the space provided. Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided. Where more than 3 applicants are to be named, the names and address of the fourth and any further applicants should be given on a separate sheet attached to this form together with the signature of each of these further applicants.

3. The declaration of priority at paragraph III should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under the Patents (Convention Countries) Order] should be identified and the name of that country should be entered in the space provided.

4. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph IV should be completed by marking the 'YES' Box in the declaration (a) and the 'NO' Box in the alternative statement (b). Where this is not the case, the 'NO' Box in declaration (a) should be marked and a statement will be required to be filed on Patents Form 8.

5. If the applicant has appointed an agent to act on his behalf, the agent's name should be indicated in the spaces available at paragraph V.

6. An address for service in Singapore to which all documents may be sent must be stated at paragraph VI. It is recommended that a telephone number be provided if an agent is not appointed.

7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified at paragraph VII and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(*a*), they should also indicate the date on which the earlier application was amended.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' Box at paragraph VIII should be marked. Otherwise the 'NO' Box should be marked.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' Box at paragraph IX should be marked. Otherwise the 'NO' Box should be marked.

10. Attention is drawn to rules 90 and 105 of the Patent Rules. Where there are more than 3 applicants, see also Note 2 above.

11. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least 2 months after the application has been filed in Singapore.

For Official Use

Application Filing Date: / /

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Fee received on : / /

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FLEXIBLE BALL GRID ARRAY CHIP SCALE PACKAGES AND METHODS OF FABRICATION

TECHNICAL FIELD

Field of the Invention: The present invention relates to methods and apparatus for packaging single and multiple semiconductor dice to provide an array-type pinout. In particular, the present invention relates to methods and apparatus for packaging semiconductor dice in the form of chip scale, ball grid array packages.

Background Art: Semiconductor dice are conventionally packaged individually in plastic or, less commonly, ceramic packages. Packaging supports, protects, and dissipates heat from the semiconductor die and provides a lead system for power and signal distribution to and from the semiconductor die. The die package also facilitates burn-in and other testing of each semiconductor die prior to and after its assembly with higher level packaging.

One type of integrated circuit (IC) or semiconductor die package is referred to as a "chip scale package", "chip size package", or merely CSP. These designations arise largely from the physical dimensions of the package, which are only nominally larger than the actual dimensions (length, width and height) of the unpackaged semiconductor die. Chip scale packages may be fabricated in "uncased" or "cased" configurations. Uncased chip scale packages do not include an encapsulation or other covering of the sides of semiconductor die extending between the active surface and back side thereof, and thus exhibit a "footprint" (peripheral outline) that is substantially the same as that of an unpackaged semiconductor die. Cased chip scale packages have encapsulated or covered sides and thus exhibit a peripheral outline that is slightly larger than that of an unpackaged semiconductor die. For example, a surface area of a footprint for a conventional cased chip scale package may be up to about 1.2 times that of the bare semiconductor die contained within the package.

A chip scale package may typically include an interposer substrate bonded to the active surface of the semiconductor die. The interposer substrate may include traces extending to contacts for making external electrical connections to the semiconductor die of the chip scale package. The interposer substrate for a chip scale package may comprise a flexible material, such as a polymer (i.e., polyimide) tape, or a rigid material,

such as silicon, ceramic, glass or FR-4 or other fiberglass laminate. The external contacts for one type of chip scale package include solder balls or other discrete conductive elements protruding from the package and arranged in an array. Such a design is termed a "ball grid array" (BGA), or a "fine ball grid array" (FBGA) for such an array having a very closely spaced, or pitched, array of discrete conductive elements. BGA and FBGA packaging provides the capability for a high number of inputs and outputs (I/Os) for a chip scale package, several hundred I/Os being easily achieved if necessary or desirable.

In integrated circuit packaging surface mount technology, such as so-called "vertical surface mount packages" or "VSMP" technology, has also provided an increase in semiconductor die density on a single carrier substrate or circuit board. This results in more compact designs and form factors and a significant increase in integrated circuit density. However, many VSMP designs are somewhat costly to implement and require fairly complex and sophisticated carrier substrates. In addition, for some applications, the relatively large distance of protrusion of the VSMPs above the carrier substrate unacceptably limits the number of carrier substrates which may be inserted transversely in adjacent slots of a higher level packaging substrate, such as a PC motherboard.

Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. As new generations of integrated circuit products are released, the volume and thus cost of components used in packaging tends to decrease due to advances in packaging technology, even though the functionality (memory capacity and speed, processor speed, etc) of the packaged end products increase. For example, on the average, there is approximately a 10 percent decrease in packaging component usage for every product generation in comparison to the previous generation exhibiting equivalent functionality.

Chip-scale packages are thus of current interest in modern semiconductor packaging as a method for reducing the package size and cost. Further, the industry has responded to the limited space or "real estate" available for mounting semiconductor dice on a carrier substrate by vertically stacking two or more semiconductor dice, the I/Os to the carrier substrate often being provided between the lowermost semiconductor

die and carrier substrate within the footprint of the stack. Therefore, it would be advantageous to provide a method and apparatus that may further reduce chip scale package size and enhance robustness of the package while at the same time reduce fabrication cost and enhance production flexibility in combination with providing a capability to stack two or more semiconductor dice of the same or different types to increase circuit density on a carrier substrate to which such a multi-die chip scale package is attached.

DISCLOSURE OF INVENTION

The present invention relates to chip scale packages exhibiting arrays of external contacts as well as to methods of fabricating such packages including, by way of example only, ball grid array chip scale packages. The present invention provides a reduced, substantially chip scale package of robust design and which provides the capability of stacking multiple semiconductor dice. The present invention also provides a capability to covert semiconductor dice exhibiting a peripheral or central bond pad I/O arrangement into array-type chip scale packages.

The chip scale package of the present invention includes a flexible, dielectric interposer substrate having portions attached to both an active surface and back side surface of at least one semiconductor die after folding about one side of a semiconductor die to sandwich the die therebetween. The interposer substrate used with the present invention includes a thin foldable or flexible dielectric material bearing circuit traces having terminal pads for connecting to the die or dice and for receiving discrete conductive elements thereon for connecting the die or dice to higher level packaging such as a carrier substrate.

In one embodiment of the invention, the interposer substrate is little more than twice the size (footprint)of a bare semiconductor die to be packaged. The interposer substrate includes a first portion substantially of die footprint size and having a first set of contacts arranged for attachment to at least some of the bond pads on an active surface of the semiconductor die and a second portion laterally offset from the first portion by a spacer portion and bearing a second set of contacts arranged in an array, the interposer substrate including circuit traces extending between the first and second

sets of contacts. A third set of contacts arranged in an array, with traces extending thereto from the first set of contacts, may optionally be located for access on the side of the first portion opposite the first set of contacts. The first set of contacts of the first portion of the interposer substrate are mechanically and electrically connected to the bond pads, which are preferably bumped with a conductive material, by any suitable technique known in the art, after which the second portion of the interposer substrate is folded or wrapped around a side edge of the semiconductor die and adhesively attached to the back side of the semiconductor die. A dielectric underfill may optionally be disposed between the first portion of the interposer substrate and the active surface of the semiconductor die. Discrete conductive elements such as, by way of example only, solder balls, may be formed on the second set of contacts lying over the back side of the semiconductor or, if the interposer substrate employs the third set of contacts, either the second of third set of contacts may be so bumped, as desired. If both second and third sets of contact are provided, multiple chip scale packages according to this embodiment of the invention may be stacked.

In another embodiment of the present invention, bond pads of a first and a second semiconductor die are bumped with conductive material and then attached face to face to respective first and second sets of contacts on opposing sides of a first portion of an interposer substrate. An underfill material may be optionally disposed between one or both of the first and second semiconductor dice and the interposer substrate. The second portion of the interposer substrate is then folded about a side of either the first or the second semiconductor die and bonded to the back side of the semiconductor die about which it is folded. The second portion of the interposer substrate includes conductively-filled through vias extending from one side of the second portion to the other and connected to the first and second sets of contacts by conductive traces extending therebetween. To avoid shorting, the second portion may be bonded to the die backside using a non-conductive adhesive. Since the vias of the second portion of the interposer substrate extend completely therethrough and provide electrical contacts at each end thereof, discrete conductive elements may be applied thereto regardless of which semiconductor die back side is adhered to the second portion.

In a variant of the second embodiment, the second portion of the interposer substrate is extended in length and includes two longitudinally spaced second portions.

With the extended second portion, a first, second portion is folded about a side of either the first die or the back side of the second die and then bonded to the back side thereof, after which a second, second portion is wrapped around the side of the other semiconductor die and bonded to the back surface thereof. In this variant, each of the first and second, second portions carries a set of contacts so that a ball grid array may then be provided to either an upper outside surface or a bottom outside surface of the package, as desired. This variant of the second embodiment of the invention also provides the capability of stacking multiple chip scale packages.

Methods of fabricating the chip scale packages of the present invention, as well as assemblies of higher level packaging incorporating the inventive packages are also contemplated as being encompassed by the invention.

BRIEF DESCRIPTION OF DRAWINGS

The method and apparatus of the present invention will be more fully understood from the detailed description of the invention taken in conjunction with the drawings, wherein:

FIGs. 1(a) - 1(g) illustrate a method of making a flexible single semiconductor die chip scale package in accordance with a first embodiment of the present invention, in which FIG. 1(a) is a simplified perspective view and FIGs. 1(b) - 1(g) are simplified cross-sectional views;

FIGs. 2(a) - 2(b) are simplified cross-sectional views of the first embodiment, illustrating a flexible single semiconductor die chip scale package stacked with one or more other flexible single semiconductor die chip scale packages, in accordance with the present invention;

FIGs. 3(a) - 3(e) are simplified cross-sectional views of a second embodiment, illustrating a method of making a flexible multiple semiconductor die stack chip scale package, in accordance with the present invention; and

FIGs. 4(a) - 4(b) are simplified cross-sectional views of an alternative to the second embodiment, illustrating a method for making a flexible multiple semiconductor die stack chip scale package that is stacked with another flexible multiple semiconductor die stack chip scale package, in accordance with the present invention.

BEST MODE OR MODES FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will be hereinafter described with reference to the accompanying drawings. It should be understood that these illustrations are not to be taken as actual views of any specific apparatus or method of the present invention, but are merely exemplary, idealized representations employed to more clearly and fully depict the present invention than might otherwise be possible. Additionally, elements and features common between the drawing figures retain the same numerical designation.

A method and apparatus of a first embodiment of the present invention are shown in FIGs. 1(a) - 1(d). FIG. 1(a) depicts a simplified, exploded perspective view of a semiconductor die 110 and a superimposed interposer substrate 130 prior to being mutually attached. The semiconductor die 110 may include a semiconductor substrate comprising a singulated semiconductor die or a plurality of unsingulated dice (also known in the art as a "partial wafer"). The semiconductor substrate may comprise, for example and not by way of limitation, silicon, gallium arsenide, indium phosphide or other semiconductor material known in the art. The semiconductor substrate may be severed from a larger substrate such as, for example and not by way of limitation, a silicon wafer or another substrate such as silicon-on-insulator (SOI), silicon-on-glass (SOG), etc. The semiconductor die 110 includes an active surface 112 and a back side 114, the active surface 112 including a plurality of bond pads 116p bearing electrically conductive bumps 116b. The bond pads 116p may be centrally located as shown in FIG. 1(a) in one or more rows, or may be peripherally located along one or more edges of active surface 112, as known in the art. In addition, other bond pad arrangements may be easily accommodated.

Bumps 116b preferably comprise, but are not limited to, conductive pillars, columns, or balls. The material of conductive bumps 116b may include, but is not limited to, any known suitable metals or alloys thereof, such as lead, tin, copper, silver or gold. Conductive or conductor-filled polymers may also be employed, although gold and PbSn solder bumps are currently preferred. The bumps 116b may be of uniform characteristics throughout or include, for example, a core of a first material (including a nonconductive material) having one or more conductive layers of other materials thereon. The bumps 116b, depending upon the material or materials employed therefor,

may be formed using an evaporation process, a C4 process, electroplating, electroless plating, laser bonding, or any other process as known to one of ordinary skill in the art.

The interposer substrate 130 may be a flexible dielectric tape or a ribbon type laminate structure having a first surface 132 and a second surface 134, the second surface 134 including electrical contacts thereon in the form of ball pads 135. The ball pads 135 may be formed of any suitable conductive material such as gold or tin/lead solder, the material being selected for compatibility with that of discrete conductive elements to be subsequently formed thereon. The interposer substrate 130 comprises a first portion 136 and a second, laterally offset portion 138 spaced from first portion 136 by spacer portion 140 defined between fold lines 142. Both first portion 136 and second portion 138 may have ball pads 135.

The interposer substrate 130 may be formed from any known substrate materials and is preferably formed of, by way of example, a laminated polymer material and, more specifically, a polyimide or other thermoset polymer film. In a preferred embodiment, the interposer substrate 130 may be ultra-thin with any suitable thickness, but preferably in the range between about 70 um and about 90 um.

FIG. 1(a) also illustrates a cut-out from the interposer substrate 130 depicting the internal electrical interconnection or trace routings therein over one of the dielectric films thereof, the other being partially removed for clarity. In particular, the ball pads 135 on the second surface 134 of the interposer substrate 130 interconnect through conductive traces 144 to corresponding bond posts 143 exposed on the first surface 132 of first portion 136. Each bond post 143 is electrically connected and rerouted by way of a corresponding trace 144 to two corresponding ball pads 135 on the second surface 134 of the carrier substrate 130, one on first portion 136 and one on second portion 138. Traces 144 may be formed by masking and etching a conductive film, such as copper, on one of the dielectric films, by printing using conductive ink, or otherwise as known in the art. Bond posts 143 are formed of a conductive material compatible for bonding with bumps 116. Although actually sandwiched between the two dielectric films of interposer substrate 130, traces 144 are shown partially revealed from the side in FIGS. 1(b) and 1(c) and partially in broken lines to better illustrate their extensions from bond posts 143 to ball pads 135.

FIG. 1(b) is a simplified cross-sectional view of the semiconductor die 110 mounted to the first portion 132 of interposer substrate 130. In particular, the bumps 116 on the active surface 112 of the dies 110 are bonded to the bond posts 143 on the first surface 132 of the first attach portion 136 of the carrier substrate 130. The interposer substrate's first portion 136 is thus directly facing the active surface 112 of the semiconductor die 110 so that the second portion 138 of the interposer substrate 130 is unattached and extends freely laterally from the first portions 13. The post-to-bump bonding is preferably accomplished by means of, but is not limited to, an anisotropic conductive film (ACF), an anisotropic conductive paste (ACP), a thermal compression (TC) bonding process or a thermosonic (TS) bonding process.

A dielectric filler material 146, commonly termed an "underfill" material, may be disposed in the gap 148 between active surface 112 and first surface 132 of first portion 136. Such may be particularly desirable if TC or TS bonding is employed, whereas ACF or ACP may be applied across the entire interface between active surface 112 and first surface 132. The methods employed to apply the filler material 146 to the gap 148 may include, but are not limited to, gravity dispensing, pressure injecting, combinations of pressure and vacuum to draw the material 146 into gap 148 and other suitable techniques known in the For example, filling the gap 148 may be accomplished by applying the filler material 146 from a dispenser, approximate either one side or two adjacent sides of the die 110. The filler material 146 may be self-curing through a chemical reaction, or a cure accelerated by heat, ultraviolet light or other radiation, or other suitable means in order to form a solid mass bonded to active surface 112 and first surface 132 of first portion 136.

FIG. 1(c) is a simplified cross-sectional view of the semiconductor die 110 mounted by active surface 112 to the interposer substrate 130 and having an adhesive material 152 on the back side 114. The adhesive material 152 may be applied to back side 114 of the semiconductor die 110 subsequent to attaching the interposer substrate 130 to the die's active surface 112 or may be applied to overly the back surface 114 at the wafer level or after dicing the wafer into individual or multiple semiconductor die/dice and before attachment to interposer substrate 130. The adhesive material 152 applied may be a double-sided adhesive tape, the outer layer of adhesive

facing away from back side 114 being covered with a protective layer until adherence is required.

FIG. 1(d) is a simplified cross-sectional view of the interposer substrate 130 mounted to both the active surface 112 and the back side 114 of the semiconductor die 110. After the die 110 and first portion 136 of the interposer substrate 130 are mounted and the adhesive material 152 has been applied to the back side114 of the semiconductor die 110, the flexible interposer substrate 130 is folded along fold lines 142 and wrapped around a side 154 of the semiconductor die 110 (as shown by the arrow in FIG. 1(d)) so that the extended second portion 138 of interposer substrate 130 may be adhesively attached to the back side 114 of the semiconductor die 110 via the adhesive material 152 with the spacer portion 140 of interposer substrate 130 lying over side 154 of semiconductor die 110. In this manner, the first portion 136 and the second portion 138 of the interposer substrate 130 are respectively attached to the active surface 112 and the back side 114 of the semiconductor die 110 to provide a wrapped die 160. In this manner, the interposer substrate 130 sandwiches the semiconductor die 110 to substantially overlie the active surface 112, back side 114 and edge 154. Wrapped die 160 includes a first and a second outside surface 162 and 164, respectively, each outside surface 162 and 164 comprising second surface of interposer substrate 130 and exhibiting an array of ball pads 135 thereon.

As shown in FIGs. 1(e) and 1(f), discrete conductive elements 172 may be applied to or formed on either the first outside surface 162 (FIG. 1(e)) and/or the second outside surface 164 (FIG. 1(f)) of the wrapped die 160 to complete chip scale package 170. The discrete conductive elements 172 are arranged in a two-dimensional array, commonly known as a ball grid array or BGA, corresponding to the array pattern of ball pads 135 to which conductive elements 172 are bonded so as to provide external electrical connections (I/Os) for the wrapped die 160. The array may comprise rows and columns of conductive elements 172, one or more concentric circles or rectangles of bumps, and may be highly populated as illustrated herein or comprise an open array with fewer elements and large pitch (spacing) between the discrete conductive elements 172. The conductive elements 172 may comprise balls, bumps, pillars, columns or other suitable structures. The conductive elements may include, but are not limited to, any known conductive metal or alloys thereof, such as lead, tin, copper, silver, or gold as

well as conductive or conductor-filled polymers. The conductive elements 172 may include a core of a first material (including non-conductive materials having one or more conductive layers thereon).

As shown in FIG. 1(g), the chip scale package 170 with conductive elements 172 attached thereto may then be mounted to a carrier substrate such as a printed circuit board (PCB) 182 or any other substrate or other higher level packaging, such as an interposer or another semiconductor die, the conductive elements 172 providing mechanical and electrical connections to terminal pads (not shown) of the other substrate. The conductive elements 172 provide a standoff between the wrapped die 160 and, for example, PCB 182. The chip scale package 170 may thus be bonded to terminal pads or trace ends of the PCB 182 by, for example, reflowing (in the case of solder) or curing (in the case of conductive or conductor-filled polymers) to form an electronic assembly as known in the art.

Once the chip scale package 170 is mounted to the PCB 182 via the conductive elements 172, a dielectric filler material 184 may then be optionally be provided therebetween as known in the art for enhanced securement of chip scale package 170 and to preclude shorting between conductive elements 172.

In addition, a nonconductive layer or film 186 may optionally be applied to overlie the outside surface 162 or 164 of the wrapped die 160 having no conductive elements 172 thereon. The insulating layer or film 186 prevents electrical shorting between exposed, laterally adjacent ball pads 135 which, for clarity, are not shown in FIG. 1(g) as they are covered by film 186. This insulating layer or film 186 may be applied subsequent to, or preferably prior to, mounting the wrapped die 160 to the PCB 182.

It will be appreciated by those of ordinary skill in the art that the above described first embodiment of the chip scale package of the present invention provides an extremely thin package offering the flexibility of bumping either the active surface or back side of a semiconductor die. Thus, a so-called "mirror" die (i.e., a die having a mirror image I/O array to another, similar die) may be easily formed without retooling. It is further appreciated that the minimized height of the chip scale package of the present invention is accomplished by easily manipulating a preformed, ultra thin, flexible interposer substrate to provide the wrapped die rather than through complex and

expensive alterations in the die fabrication process. The present invention may be used to provide a robust chip scale package with a minimized height or thickness of as little as 0.85 mm. The present invention may substantially prevent potential damage to the semiconductor die during handling, assembly with a carrier substrate and testing of the resulting assembly, such as a memory module. During operation, the present invention may substantially protect the semiconductor die from environmental concerns since the interposer substrate is wrapped around both the active surface and back side of the die.

FIGs. 2(a) and 2(b) show simplified cross-sectional views of multiple CSP's of the present invention as a stacked assembly. The stacking is accomplished by mounting the conductive elements 172 of one BGA die to corresponding ball pads 135 on the first or second outside surface 162 and 164 of a wrapped die 160 of chip scale package 170. Multiple chip scale packages 170 may be stacked in a similar manner to significantly multiply the integrated circuit density, the bottom chip scale package 170 being mounted to a PCB or any other carrier substrate or higher level packaging. FIGs. 2(a) and 2(b) depict stacking the chip scale packages 170 in different orientations corresponding to the different orientations shown and described in association with FIGs. 1(e) and 1(f), respectively. It will be appreciated that different types of dice may be stacked, for example a logic die on a memory die, or an SRAM die on a DRAM die. Alternatively, a plurality of memory dice may be stacked to effectively provide a virtual, single stack memory "module" of enhanced memory capacity or memory and logic dice may be stacked on a microprocessor die to provide a chip scale computer. Further, another BGA die of different design may be stacked on a chip scale package of the present invention and bonded to exposed ball pads thereon.

The decision of proceeding to bump the first or second outside surface 162, 164 of the wrapped die 160 may be made just prior to adding the conductive elements 172 to complete the chip scale package 170, providing additional flexibility in the planning and production of the chip scale package 170 of the present invention. Furthermore, should the orientation of the wrapped die 160 need to be reversed or flipped, this may easily be achieved by removing the conductive balls 172 from ball pads 135 on one surface of the wrapped die 160 and adding the conductive balls 172 to the ball pads 135 on the opposite surface of the wrapped die 160.

A method and apparatus of a second embodiment of the present invention is shown in FIGs. 3(a) - 3(e). The second embodiment of the present invention is similar to the first embodiment in major aspects, the second embodiment including an additional semiconductor die.

As shown in the simplified cross-sectional view in FIG. 3(a), the second embodiment includes a first and second dice 110a and 110b. The first and second dice 110a and 110b each include an active surface 112 and a back side 114 respectively and each may include conductive bumps such as (for example) solder bumps or gold stub bumps 116b formed on or attached to bond pads 116p on the active surfaces 112 thereof. As in the first embodiment, the bond pads 116p may be formed in an arrangement such as one or more rows centrally located on the active surfaces 112 or, alternatively arranged along a periphery thereof.

FIG. 3(b) is a simplified cross-sectional view of the first and second dice 110a and 110b attached to an interposer substrate 230. The first and second dice 110 may be attached to first portion 236 of interposer substrate 230 employing the same processes as discussed with respect to the first embodiment, either simultaneously or sequentially. Interposer substrate 230 is structured in a similar manner to that of interposer substrate 130, being a laminate of two dielectric films having conductive traces 144 extending therebetween. However, conductive traces 144 of interposer substrate 230 extend from metallization pads 242 to an array of conductive through vias 235 extending from a first surface 232 of interposer substrate 230 to a second, opposing surface 234.

As shown in FIG. 3(c) and 3(d), the arrangement of the second embodiment provides for the second portion 238 of the carrier substrate 230, being freely extended laterally from first portion 238 and separated therefrom by spacer portion 240 as shown in Fig. 3(b), to fold or wrap around either a side 154 of the first die 110a (FIG. 3(c)) or a side 154 of the second die 110b (FIG. 3(d)). Prior to folding the carrier substrate 230, a non-conductive adhesive material 252, such as Hitachi DF-400, Hitachi HM-122 and Lintec LE-5000X, may be applied to the back side 114 of the first or second die 110a and 110b to which second portion 238 is to be adhered. The non-conductive adhesive material 252 may be applied at any time prior to folding the carrier substrate 230 to be attached thereon, which may include applying the adhesive on the back sides 114 at the

wafer level or subsequent to dicing the wafer. Thus, the second portion 238 of the carrier substrate 230 may fold around and be adhesively attached to either the back side 114 of the first die 110a or the back side 114 of the second die 110b, to form a stacked die assembly 260.

An array of discrete conductive elements 172 may then be applied to the side of stacked die assembly 260 on the exposed outside surface 262a FIG. 3(c)) or 262b (FIG. 3(d) of the carrier substrate 230 to form a multi-die chip scale package 270. Specifically, the discrete 172 conductive elements are applied to or formed on exposed surfaces of through vias 235 of the interposer substrate 230, the exposed surfaces on the via ends comprising ball pads as in the first embodiment described above. The conductive elements 172 may be of any suitable configuration and material or materials, as previously described above. The conductive filling of the through vias 235 may be selected to be compatible with the conductive material of discrete conductive elements 172 or the exposed surfaces of the through vias 235 may be plated for better bonding with the conductive elements 172, as well known in the art. Furthermore, as shown in FIG. 3(e), a dielectric or insulating layer or film 186 may optionally be applied to the exposed back side of the first or second die 110a or 110b, depending upon which die is not covered with second portion 238 of interposer substrate 230. This insulating layer 186 may also be optionally provided at the wafer level or after the wafer is diced into individual semiconductor die. The insulating layer 186 may be provided to overlie the chip scale package 270 as a covering for physical protection of the die and to reduce the potential for shorting of the assembly in use. If the covered die is of a type wherein the back side is voltage biased, the use of insulating layer 186 is particularly desirable.

As depicted in FIG. 3(e), the chip scale package 270 may be attached to terminal pads or other conductive structures of a carrier substrate such as PCB 182 or any other higher level packaging by the array of discrete conductive elements 172. The manner of attachment is dependent upon the type of discrete conductive elements 172 employed, as described above. Also, in a similar manner to that described in the previous embodiment, the discrete conductive elements 172 provide a standoff between the stacked die assembly 260 and the PCB 182, into which a dielectric filler material may be introduced as well known in the art.

Thus, it is apparent that the second embodiment of the chip scale package of the present invention encompasses a novel and unobvious method and apparatus and provides the capability to fabricate an ultra thin, stacked multiple die, chip scale package of no more than approximately 1.0 mm in height. Further, the option of attaching the second portion 238 of the interposer substrate 230 to the back side of either the first or second die 110a 0r 110b may be determined just prior to actually attachment thereof, providing additional flexibility in the planning, production and in-line balancing of the chip-scale package of the present invention. As with the first embodiment, the dual attachment capability facilitates the fabrication of mirror-image packages.

In FIGs. 4(a)-4(b), a variant of the second embodiment is illustrated. Previously identified components and features are identified by the same reference numerals. This variant is similar to the second embodiment except that the interposer substrate 330 is extended in length and comprises a first portion 336, first spacer portion 340a and two second portions 338a and 338b separated by a second spacer portion 340b. With this configuration, the second portions 338a and 338b may be wrapped about the back sides 114 of both the first die 110a and the second die 110b by folding the two second portions 338a and 338b about the side 154 of one of the dice 110, covering that side 154 with the first spacer portion 340a, securing second portion 338a on the back side 114 of the one of the dice 110, then covering the two adjacent sides 154 of the dice 110 on the other side of the assembly with second spacer portion 340b and securing second portion 338b to the back side 114 of the other die 110 to form a stacked die assembly 360. Both second portions 338a and 338b may include an array of ball pads 135 to which traces 144 (not shown) extend from contact points with the bond pads of the dice 110. This variant of the second embodiment thus provides both an upper outside surface 362 and a lower outside surface 364, on which discrete conductive elements 172 may be placed in an array corresponding to the pattern of ball pads 135. As in the second embodiment, the stacked die assembly 360 with discrete conductive elements 172 forming a chip scale package 370 may then be attached to terminal pads or other contacts of a carrier substrate such as a printed circuit board 182 or any other higher level packaging. However, in this variant of the second embodiment, the chip scale package 370 may be stacked with one or more other chip scale packages bearing 370 discrete conductive elements 172 since the interposer

substrate 330 wraps around both the upper and bottom outside surface 362 and 364, to enable electrical connection with another stacked die assembly 360. It will also be readily appreciated by those of ordinary skill in the art that another flip-chip type die or a stacked die assembly of different design may be connected to a stacked die assembly, and that dice with different functions may be combined into a stacked die assembly or connected thereto. Thus, this variant of the second embodiment provides even further advantages of increasing integrated circuit density.

It will be understood and appreciated by those of ordinary skill in the art that a die having a first arrangement of bond pads on an active surface thereof (for example, a central row), may be combined into a dual die assembly with a second, different arrangement of bond pads (for example, two peripheral rows on opposing edges of the active surface) through appropriate configuring of the interposer substrate contacts and traces. Further, different die generations, i.e., one or more "shrinks" of a basic design, may be combined into an assembly.

While the present invention has been disclosed in terms of a certain preferred embodiments and alternatives thereof, those of ordinary skill in the art will recognize and appreciate that the invention is not so limited. Additions, deletions and modifications to the disclosed embodiments may be effected without departing from the scope of the invention as claimed herein. Similarly, features from one embodiment may be combined with those of another while remaining within the scope of the invention.

CLAIMS

What is claimed is:

1. A semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side and a side extending transversely therebetween;

a plurality of bond pads over the active surface in a first arrangement; and

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion and including a first plurality of electrical contacts on the first side of the first portion connected to the bond pads of the plurality and communicating through conductive traces with at least a second plurality of electrical contacts in a second arrangement different from the first arrangement on the second side of the second portion;

wherein the first portion of the interposer substrate extends and is secured over the active surface of the first semiconductor die, the second portion is secured over the back side thereof and the spacer portion extends over the side thereof.

2. The semiconductor die assembly of claim 1, further including discrete conductive elements disposed over the contacts of the second plurality and projecting transversely therefrom.

3. The semiconductor die assembly of claim 2, wherein the second arrangement comprises a two-dimensional array.

4. The semiconductor die assembly of claim 1, further including a third plurality of electrical contacts on the second side of the first portion in a third arrangement in communication with the first plurality of electrical contacts through conductive traces.

5. The semiconductor die assembly of claim 4, wherein the third arrangement

is a mirror image of the second arrangement.

6. The semiconductor die assembly of claim 5, wherein the second arrangement comprises a two-dimensional array.

7. The semiconductor die assembly of claim 4, further including discrete conductive elements disposed over the contacts of the third plurality and projecting transversely to the active surface of the first die.

8. The semiconductor die assembly of claim 4, further including discrete conductive elements disposed over the contacts of one of the second plurality and the third plurality and projecting transversely therefrom.

9. The semiconductor die assembly of claim 8, further including a second die disposed over the first die and in electrical communication with the first die through another of the second plurality and the third plurality of contacts.

10. The semiconductor die assembly of claim 9, wherein the second die includes discrete conductive elements projecting transversely therefrom, by which the electrical communication with the first die is effected.

11. The semiconductor die assembly of claim 10, wherein the second die is configured substantially identical to the first die.

12. The semiconductor die assembly of claim 1, further including an underfill material disposed between the active surface of the first die and the first side of the first portion of the interposer substrate.

13. The semiconductor die assembly of claim 1, further comprising an adhesive layer over the back side of the first die securing the second portion of the interposer thereto.

14. The semiconductor die assembly of claim 1, wherein the first and second portions of the interposer substrate are each of a length and width substantially corresponding to a length and width of the first die.

15. A semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side, a side extending transversely therebetween and a plurality of bond pads over the active surface in a first arrangement;

a second semiconductor die having an active surface, an opposing back side, a side extending transversely therebetween and a plurality of bond pads over the active surface in a second arrangement; and

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a first spacer portion and including:

a first plurality of electrical contacts on the first side of the first portion connected to the bond pads of the plurality of the first semiconductor die;

a second plurality of electrical contacts on the second side of the first portion connected to the bond pads of the plurality of the second semiconductor die;

a third plurality of electrical contacts on at least one of the first and second sides of the second portion and in communication through conductive traces with the first and second plurality of contacts, the third plurality of contacts being in a third arrangement differing from the first and second arrangements;

wherein the first portion of the interposer substrate extends and is secured between the first and second semiconductor dice, the second portion is secured over the back side of one of the first and second semiconductor dice with the contacts of the third plurality accessible and the spacer portion extends over the side of the one of the first and second semiconductor dice to which the second portion is secured.

16. The semiconductor die assembly of claim 15, wherein the first and second arrangements are identical.

17. The semiconductor die assembly of claim 15, wherein the second arrangement comprises a mirror image of the second arrangement.

18. The semiconductor die assembly of claim 15, wherein the third plurality of electrical contacts is exposed on both the first and second sides of the second portion.

19. The semiconductor die assembly of claim 18, wherein the electrical contacts of the third plurality comprise conductive material-filled vias extending from the first side to the second side of the second portion of the interposer substrate.

20. The semiconductor die assembly of claim 18, further comprising discrete conductive elements disposed on and projecting transversely from the accessible contacts of the third plurality.

21. The semiconductor die assembly of claim 15, further comprising discrete conductive elements disposed on and projecting transversely from the accessible contacts of the third plurality.

22. The semiconductor die assembly of claim 15, wherein the third arrangement comprises a two dimensional array.

23. The semiconductor die assembly of claim 15, wherein the second portion of the interposer substrate comprises two adjacent second portions separated by a second spacer portion, one second portion is secured over the back side of one of the first and second semiconductor dice, the other second portion is secured over the back side of another of the first and second semiconductor dice, the first space portion extends over a side of the one of the semiconductor dice and the second spacer portion extends over the side of the another of the semiconductor dice.

24. The semiconductor die assembly of claim 23, wherein the third plurality of electrical contacts is disposed on one of the two second portions.

25. The semiconductor die assembly of claim 24, further including discrete conductive elements disposed on the contacts of the third plurality and projecting transversely therefrom.

26. The semiconductor die assembly of claim 24, further comprising a fourth plurality of contacts disposed on another of the two second portions and in communication with electrical contacts of at least one of the first and second plurality through conductive traces.

27. The semiconductor die assembly of claim 26, further including discrete conductive elements disposed on the contacts of either the third plurality or the fourth plurality and projecting transversely therefrom.

28. The semiconductor die assembly of claim 27, further including at least another semiconductor die disposed over the semiconductor die assembly and in electrical communication with the semiconductor die assembly through contacts of either the third or fourth plurality having no discrete conductive elements disposed thereon.

29. The semiconductor die assembly of claim 28, wherein the at least another semiconductor die includes discrete conductive elements projecting transversely therefrom, by which the electrical communication with the semiconductor die assembly is effected.

30. The semiconductor die assembly of claim 29, wherein the at least another semiconductor die assembly comprises another multiple-die assembly.

31. The semiconductor die assembly of claim 15, further including an underfill material respectively disposed between the active surfaces of the first semiconductor die and the second semiconductor die and the first and second sides of the first portion of the interposer substrate.

32. The semiconductor die assembly of claim 15, further comprising an adhesive layer over the back side of the one of the first semiconductor die and the second semiconductor die having the second portion of the interposer secured thereto.

33. The semiconductor die assembly of claim 15, wherein the first and second portions of the interposer substrate are each of a length and width substantially corresponding to a length and width of at least one the first semiconductor die and the second semiconductor die.

34. A semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side and a side extending transversely therebetween;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion, the first portion disposed over the active surface of the first semiconductor die and the second portion disposed over the back side thereof with the spacer portion over the side thereof, the interposer substrate further including conductive traces electrically connected to the first die and extending between the first portion and the second portion to an array of discrete conductive elements projecting transversely from the back side.

35. A semiconductor die assembly comprising:

first and second semiconductor dice having mutually facing active surfaces;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion, the first portion being disposed between the first and second semiconductor dice and the second portion being secured over a back side of one of the first and second semiconductor dice with the spacer portion over a side of the semiconductor die over which the second portion is secured, the interposer further including conductive traces electrically connected to the first and second semiconductor dice and extending between the first portion and the second portion to an array of discrete conductive elements projecting from the back side of the semiconductor die to which the second portion is secured.

36. An interposer substrate for use with to at least one semiconductor die having an active surface and a back side, the interposer substrate comprising:

a flexible dielectric substrate having a first portion and a adjacent second portion separated by a spacer portion; and

a first plurality of electrical contacts on a first side of the first portion arranged to mate with bond pads of a first selected semiconductor die and connected to a second plurality of electrical contacts on a side of a second portion of the interposer substrate through conductive traces, the second plurality of electrical contacts being in a different arrangement than the first.

37. The interposer substrate of claim 36, further comprising a third plurality of

electrical contacts on a second side of the first portion, arranged to mate with bond pads of a second semiconductor die and electrically connected through conductive traces to contacts of the second plurality.

38. The interposer substrate of claim 37, further comprising a fourth plurality of electrical contacts on another side of the second portion electrically connected to the electrical contacts of the first and third pluralities through conductive traces.

39. The interposer substrate of claim 38, wherein the second and fourth pluralities of electrical contacts are connected.

40. The interposer substrate of claim 39, wherein the second and fourth contacts lie at opposing ends of conductive vias extending transversely through the second portion.

41. The interposer substrate of claim 38, wherein the second and fourth pluralities of contacts comprise two-dimensional arrays.

42. The interposer substrate of claim 41 wherein the two-dimensional arrays comprise mirror images.

43. A method for fabricating a semiconductor die assembly, the method comprising:

providing a first semiconductor die having a first surface which oppositely faces a second surface thereof and having a side between the first and second surfaces; and

attaching one side of a first portion of a substrate to the first surface, wrapping the substrate around the side and attaching a second portion of the substrate to the second surface of said at least one semiconductor die to substantially cover the first and second surfaces.

44. The method of claim 43, further comprises disposing discrete conductive elements on the second portion of the substrate.

45. The method of claim 43, further comprising:

providing a second semiconductor die having a first surface which oppositely faces a second surface thereof and having a side between the first and second surfaces thereof;

attaching another side of the first portion of the substrate to first surface of the second die.

46. The method of claim 45, wherein the attaching the first portion of the substrate to the first and second semiconductor dice is effected prior to the wrapping of the substrate.

47. The method of claim 46, further comprises disposing discrete conductive elements on the second portion of the substrate.

48. The method of claim 47, further comprising conductively connecting the semiconductor die assembly to a carrier substrate using the discrete conductive elements.

49. The method of claim 43, further comprising conductively connecting the semiconductor die assembly to a carrier substrate using the discrete conductive elements.

50. An electronic assembly, comprising:

a semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side and a side extending transversely therebetween;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion, the first portion disposed over the active surface of the first semiconductor die and the second portion disposed over the back side thereof with the spacer portion over the side thereof, the interposer substrate further including conductive traces electrically connected to the first die and extending between the first portion and the second portion to an array of discrete conductive elements projecting transversely from the back side; and

a higher level packaging structure connected to the semiconductor die assembly through the discrete conductive elements.

51. The electronic assembly of claim 50, wherein the higher level packaging structure comprises a computer.

52. An electronic assembly, comprising:

a semiconductor die assembly comprising:

first and second semiconductor dice having mutually facing active surfaces;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion, the first portion being disposed between the first and second semiconductor dice and the second portion being secured over a back side of one of the first and second semiconductor dice with the spacer portion over a side of the semiconductor die over which the second portion is secured, the interposer further including conductive traces electrically connected to the first and second semiconductor dice and extending between the first portion and the second portion to an array of discrete conductive elements projecting from the back side of the semiconductor die to which the second portion is secured; and

a higher level packaging structure connected to the semiconductor die assembly through the discrete conductive elements.

53. The electronic assembly of claim 52, wherein the higher level packaging structure comprises a computer.

ABSTRACT

FLEXIBLE BALL GRID ARRAY CHIP SCALE PACKAGES AND METHODS OF FABRICATION

A method and apparatus for increasing the integrated circuit density in a semiconductor assembly. The assembly includes a flexible interposer substrate attached to an active surface and a back side of a first die, the interposer substrate wrapping around at least one side of the first die. The assembly also includes an array of discrete conductive elements connected to bond pads of the first die through conductive traces and exposed on an exterior surface of the interposer substrate for effecting an external electrical connection. The assembly may include a second die facing the first die and attached to the interposer substrate, the interposer substrate being wrapped around either the first or second die or, alternatively, being wrapped around both the first and second die. Designate Figure 1(g).

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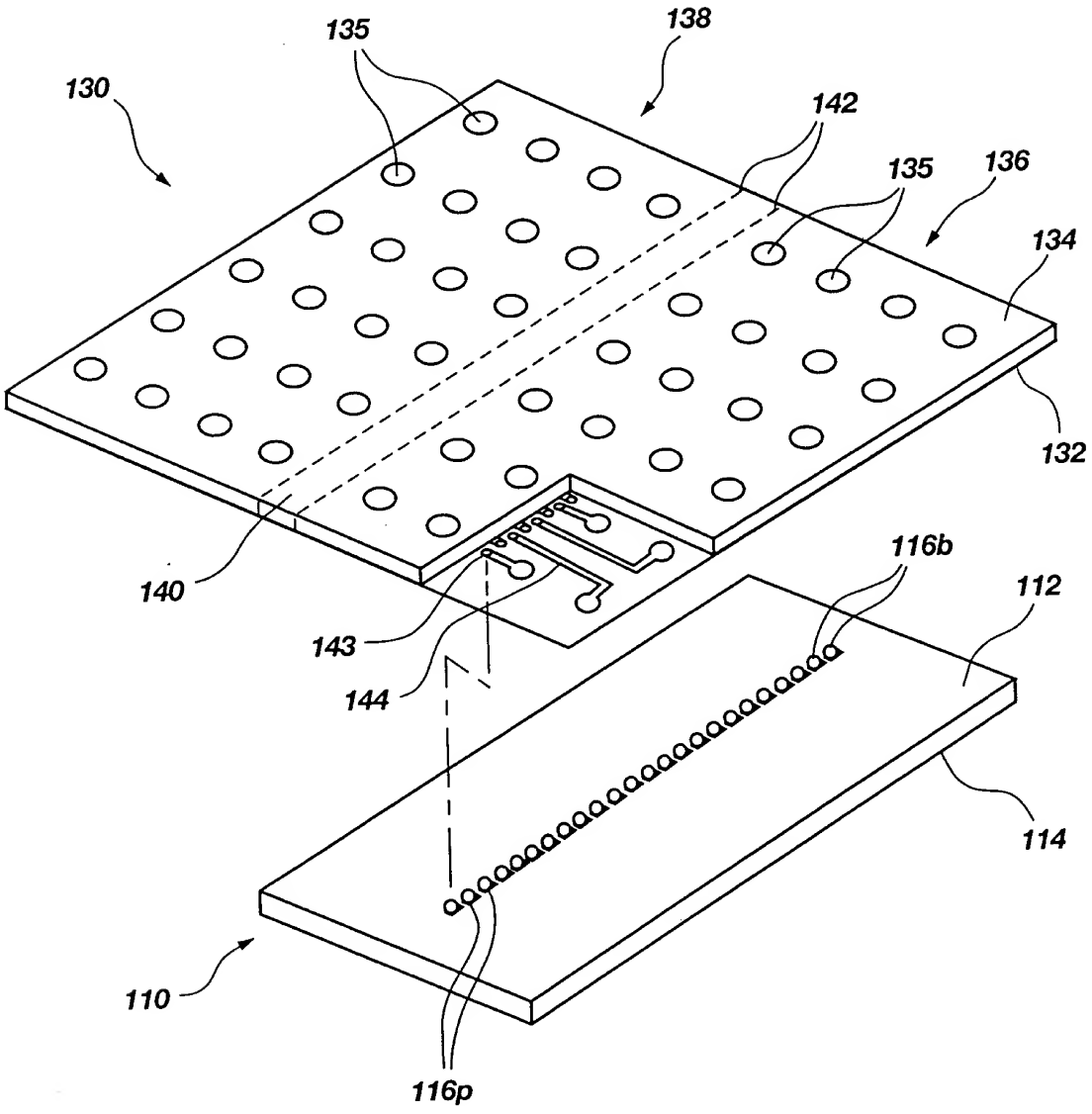
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Fig. 1(a)

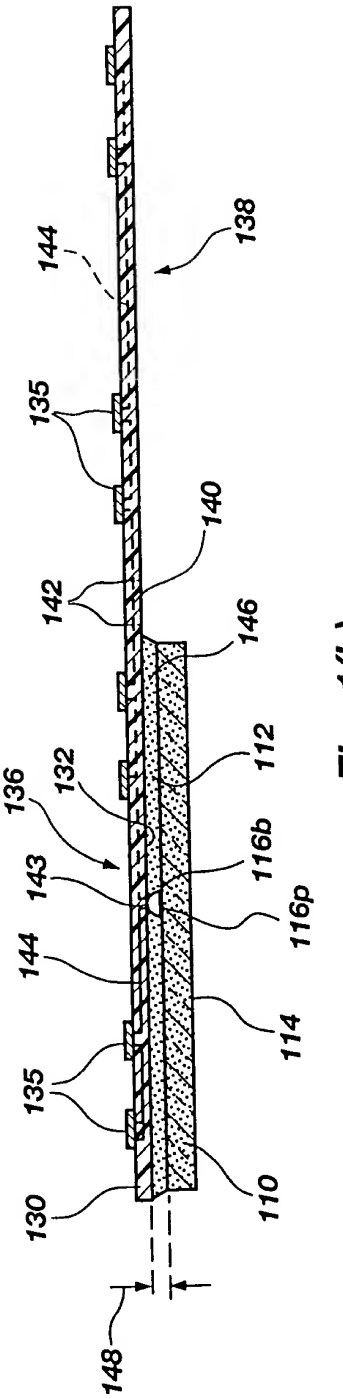
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Fig. 1(b)

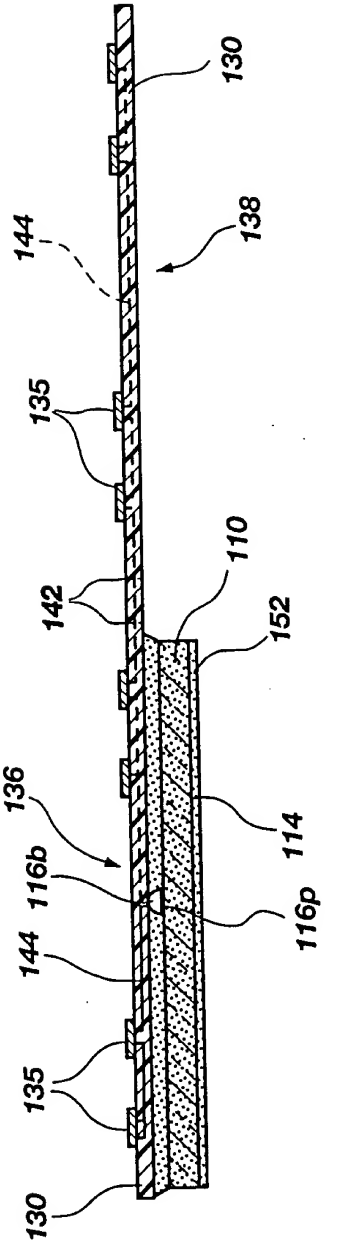
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Fig. 1(c)

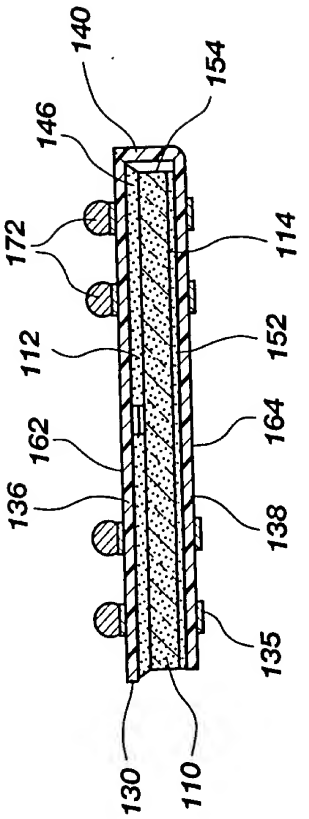

Fig. 1(e)

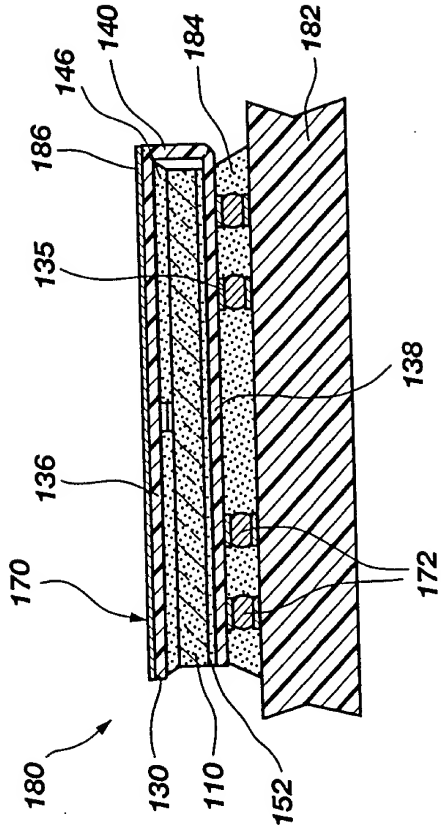

Fig. 1(g)

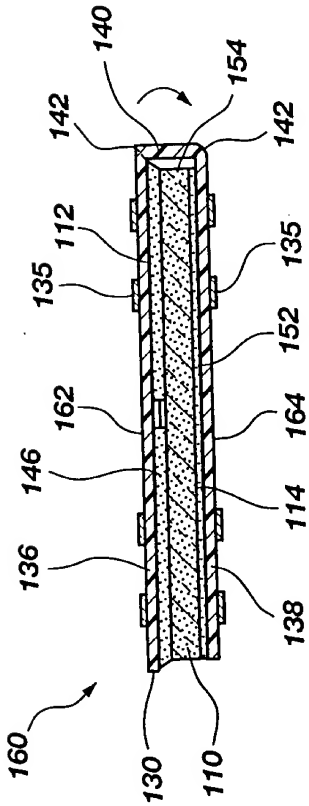

Fig. 1(d)

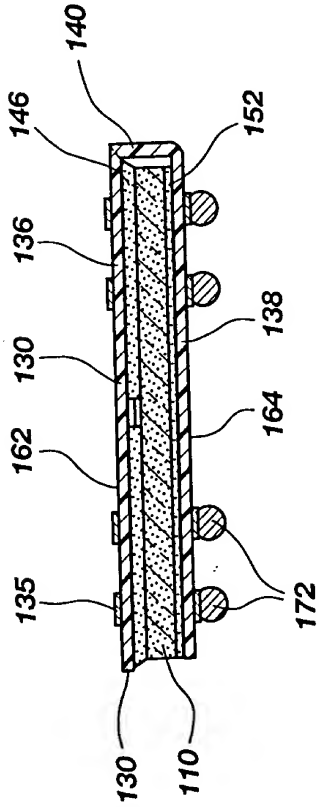

Fig. 1(f)

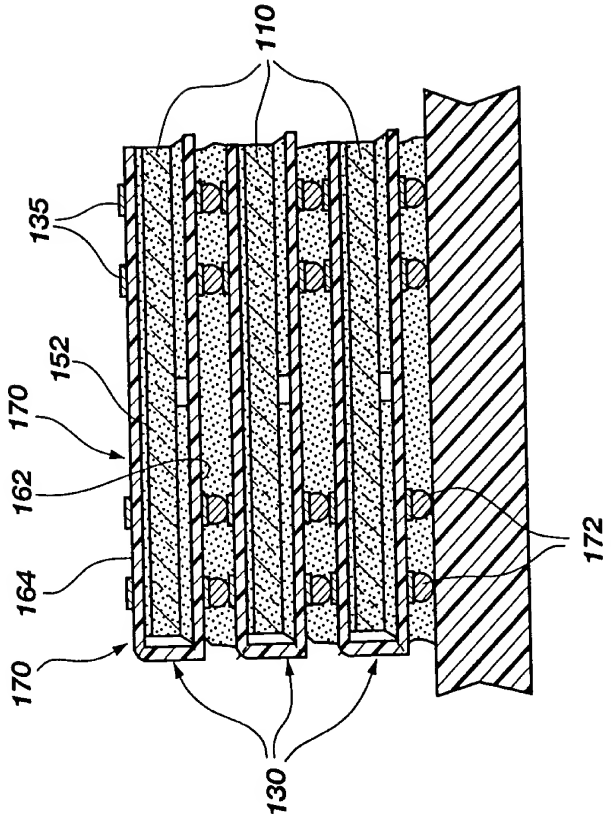
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Fig. 2(b)

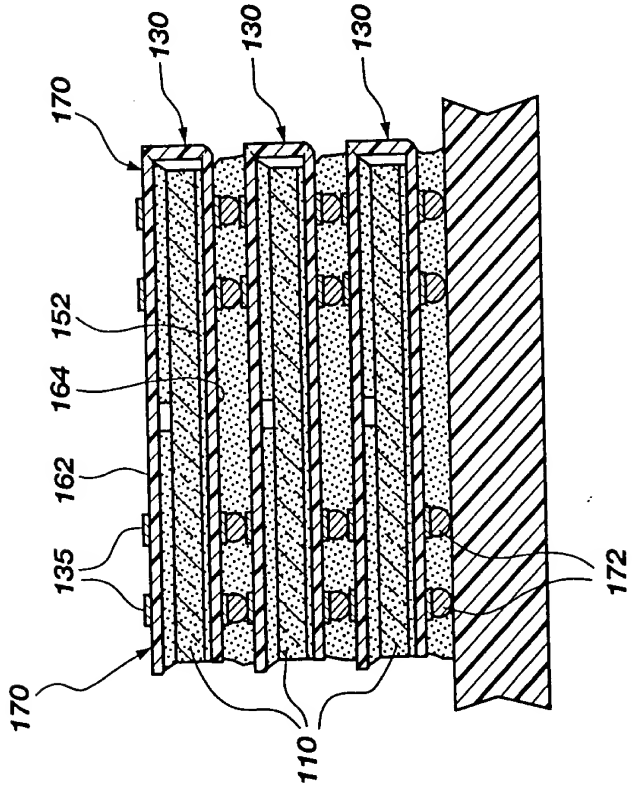
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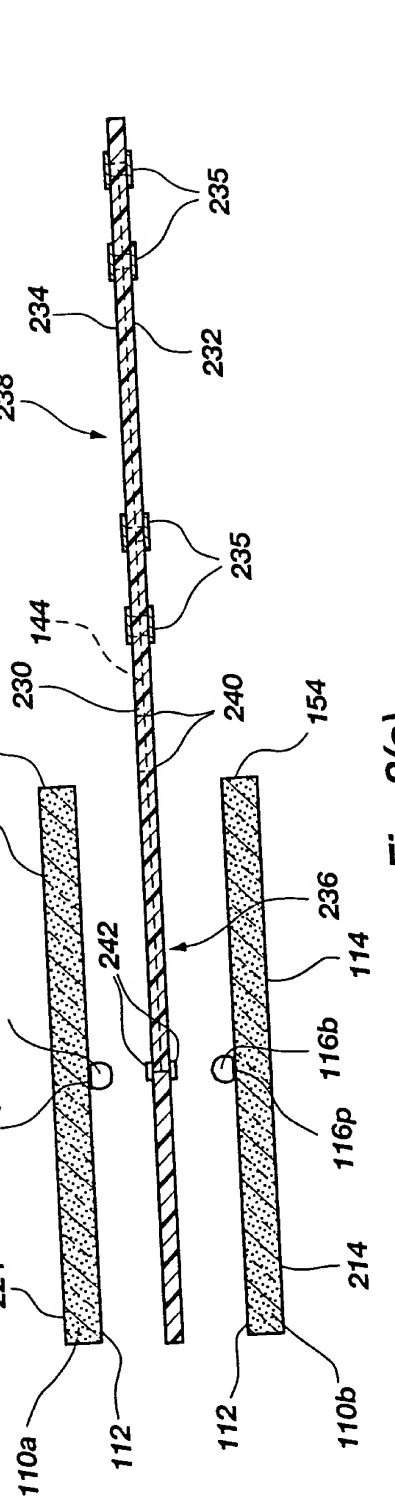
Fig. 2(a)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110b

Fig. 3(a)

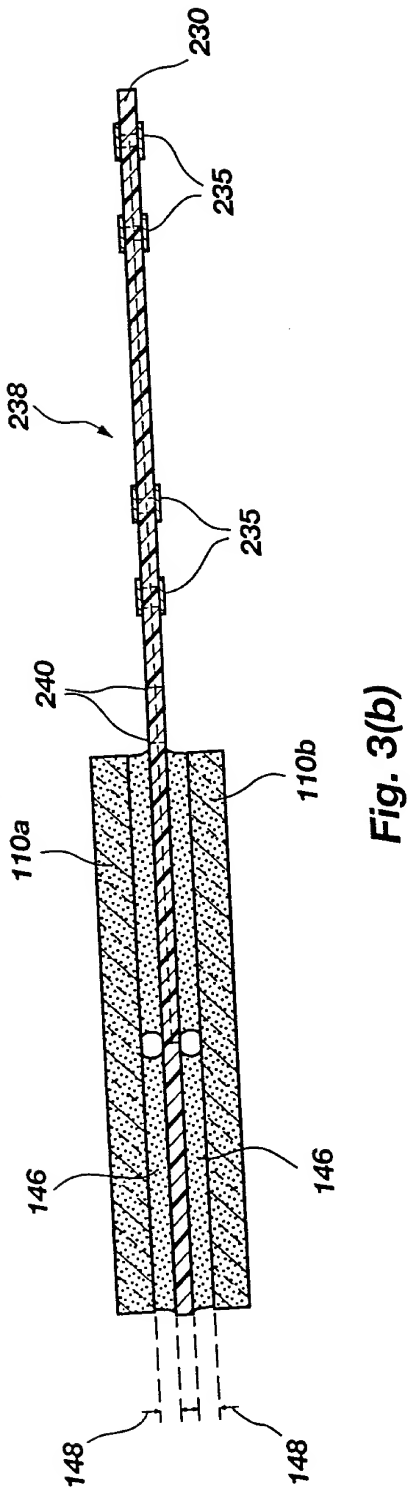
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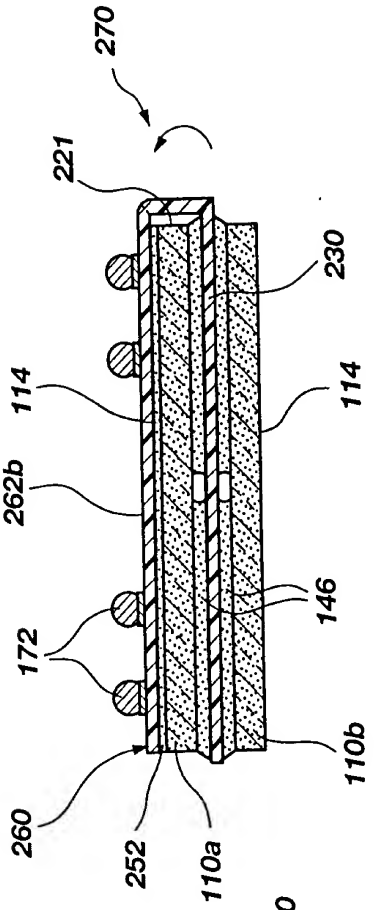
Fig. 3(b)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114
262b
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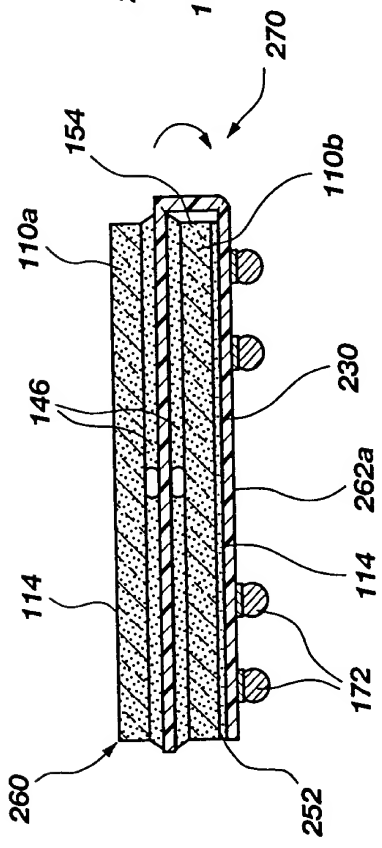
172
110b
260
252
110a

Fig. 3(d)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172
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Fig. 3(c)

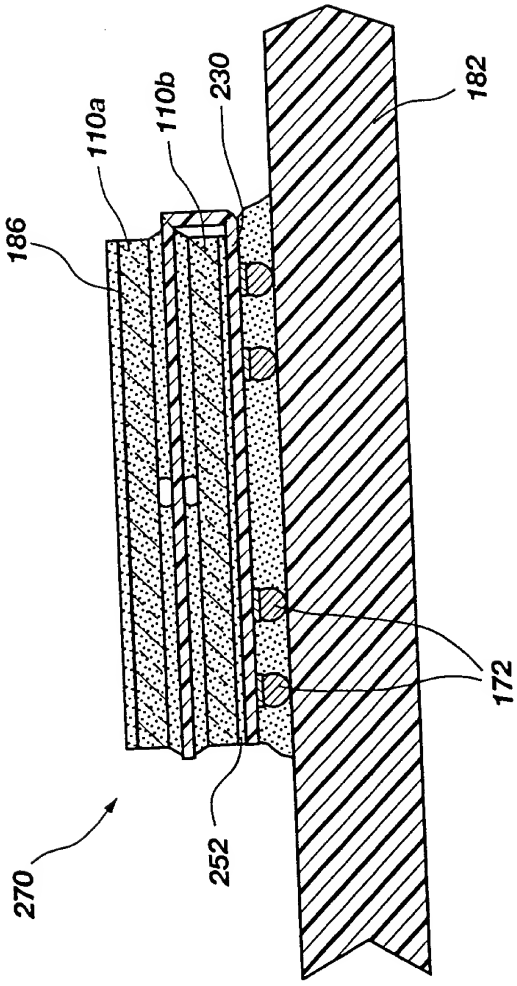

Fig. 3(e)

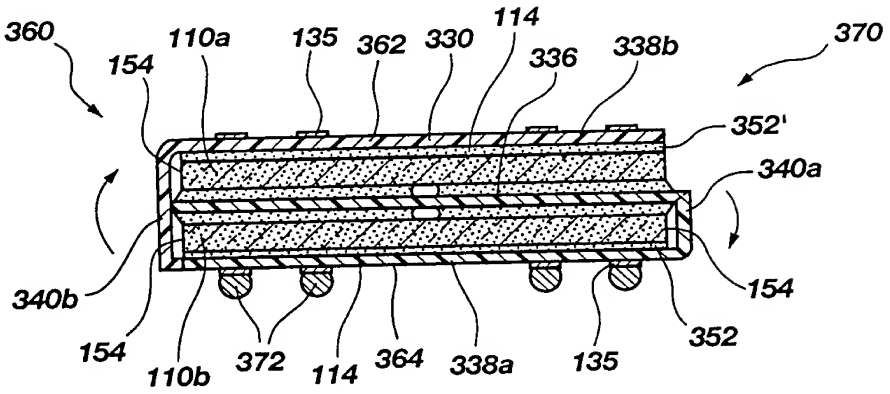
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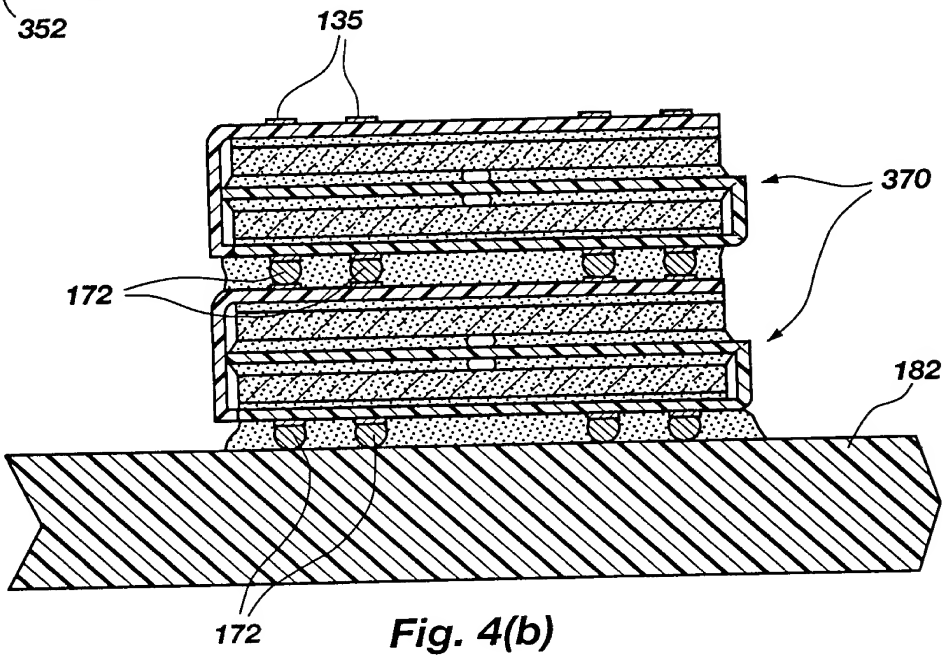
Fig. 4(a)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172

Fig. 4(b)